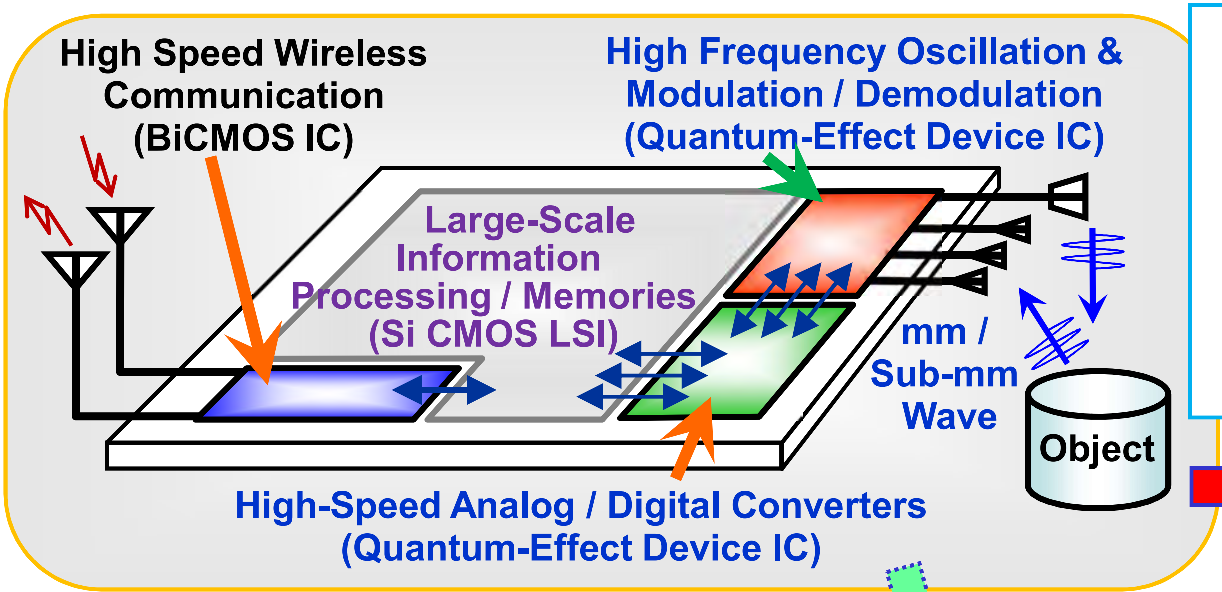
Group IV Quantum Heterointegration in Future Si LSIs



High Speed Wireless Communication (BiCMOS IC)

High Frequency Oscillation & Modulation / Demodulation (Quantum-Effect Device IC)

Large-Scale Information Processing / Memories (Si CMOS LSI)

High-Speed Analog / Digital Converters (Quantum-Effect Device IC)

Requirements of Integrated Systems for Diversification of Information Communication

- Small (Mobile)
- Low Power Consumption
- Efficient Circuit Configuration Utilizing Novel Devices

Aim of This Study:
Development of Fundamental Technologies of Quantum-Effect Devices to be integrated onto Si LSIs

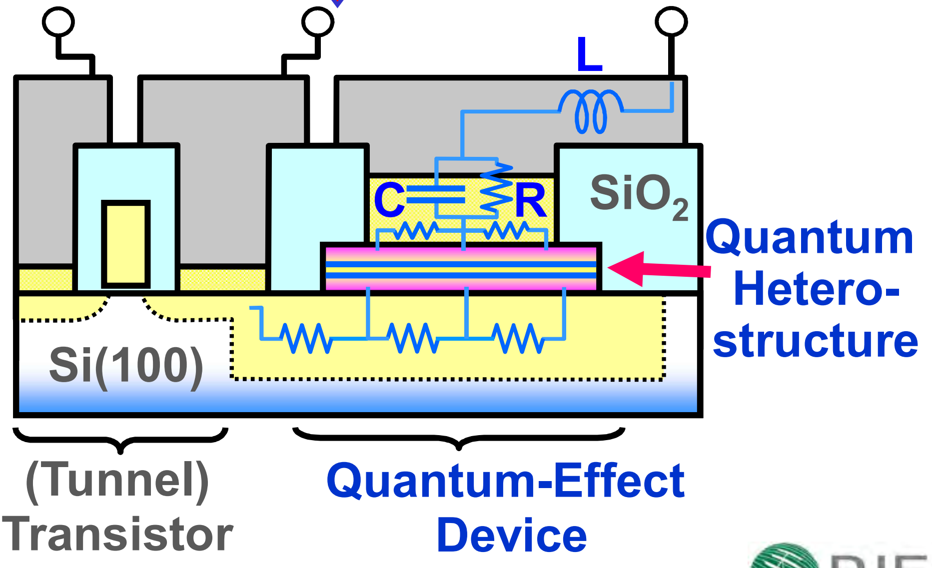
EU R&D Project: DOTSEVEN (DOTFIVE)
Towards Ultimately High-Performance of
SiGe Hetero Bipolar Transistor (HBT)
Maximum Frequency 0.7THz (0.5THz)

↓

Integration onto Si LSI（BiCMOS）

Targeted Applications:

- High-Speed Information Processing / Communication
- Radar System
- Health Care, Medical

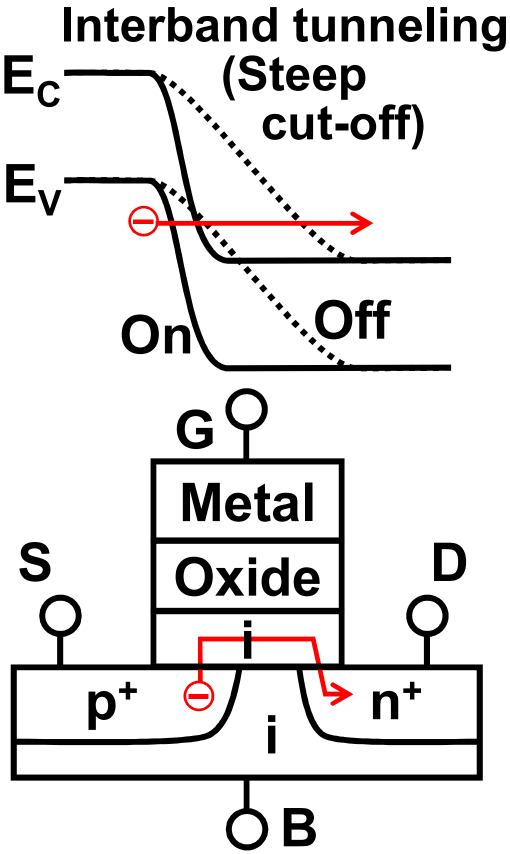


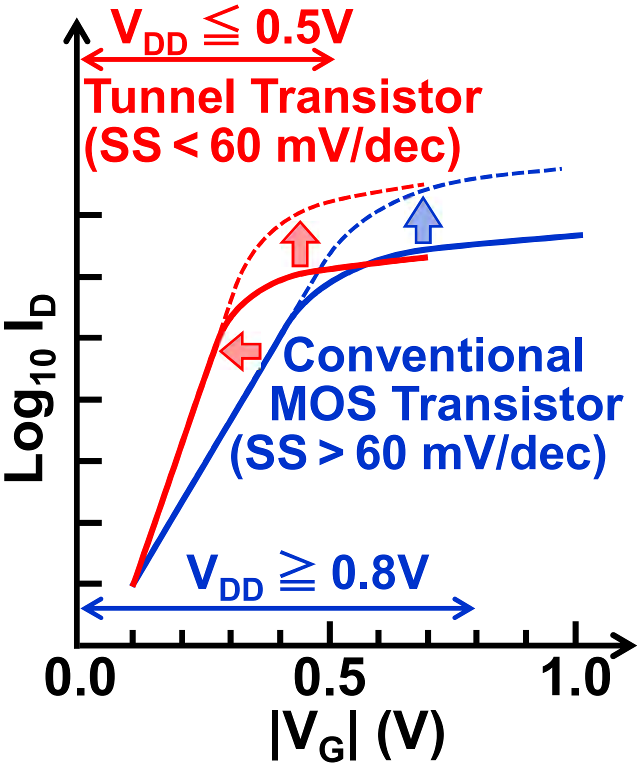
Tunnel Transistor for Low-Voltage Operation of CMOS LSI

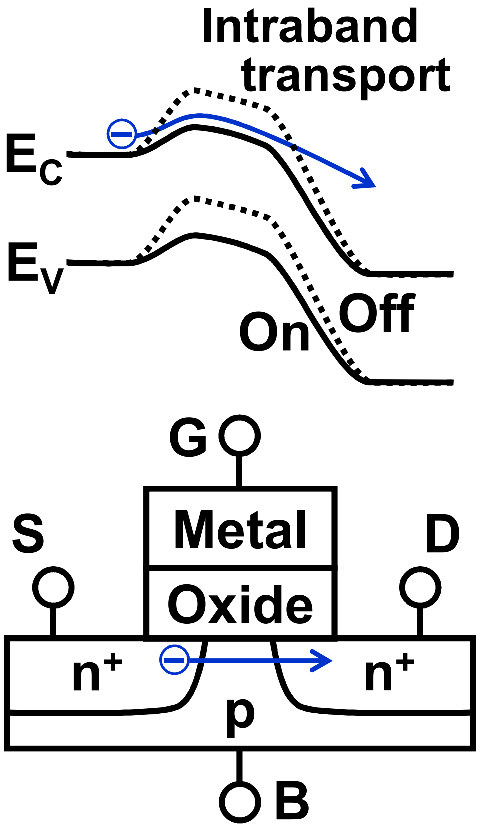
Tunnel Transistor

Breaking the Subthreshold-Swing (SS) Limit

Conventional MOS Transistor







Morita et al., IEDM Tech. Dig. (2014) 243
Morita et al., JJAP 55 (2016) 04EB06

Dynamic Power = $C\, V_{DD}^2$

Intrinsic Speed = $I_D／(C\, V_{DD})$

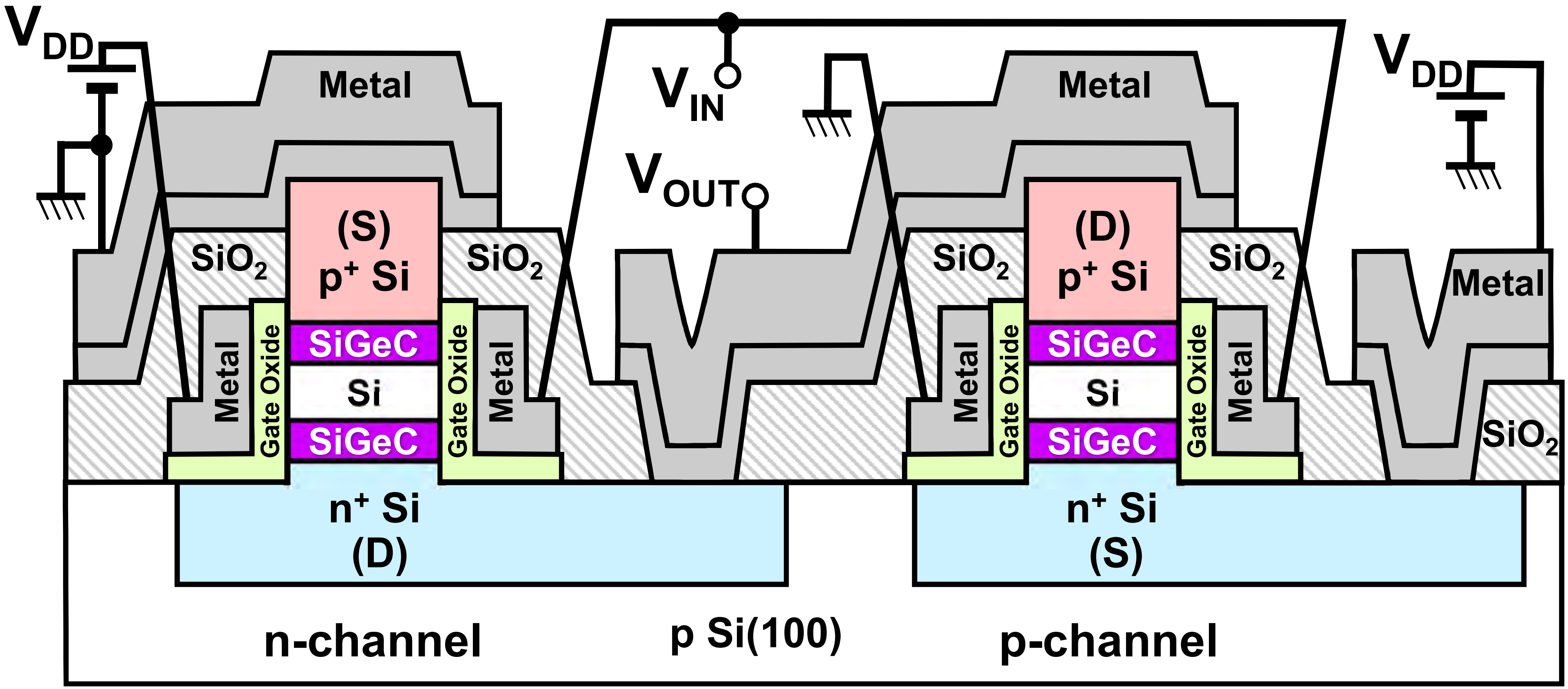
Issues for improved current drivability

- Heavy doping/diffusion control
- High-performance gate stack
- Reduction of effective bandgap by heteroepitaxy
  → Si／strained Si-Ge alloy, Ge／strained Si, Ge／Ge-Sn alloy, …

CMOS Inverter by Hetero-Tunnel Transistors (1)

Targeted Structure

- Vertical-type tunnel transistor with double sidewall gates
- Utilizing epitaxial growth of strained Si-C／Si-Ge-C alloy and Si with abrupt heterointerfaces for effective band discontinuity

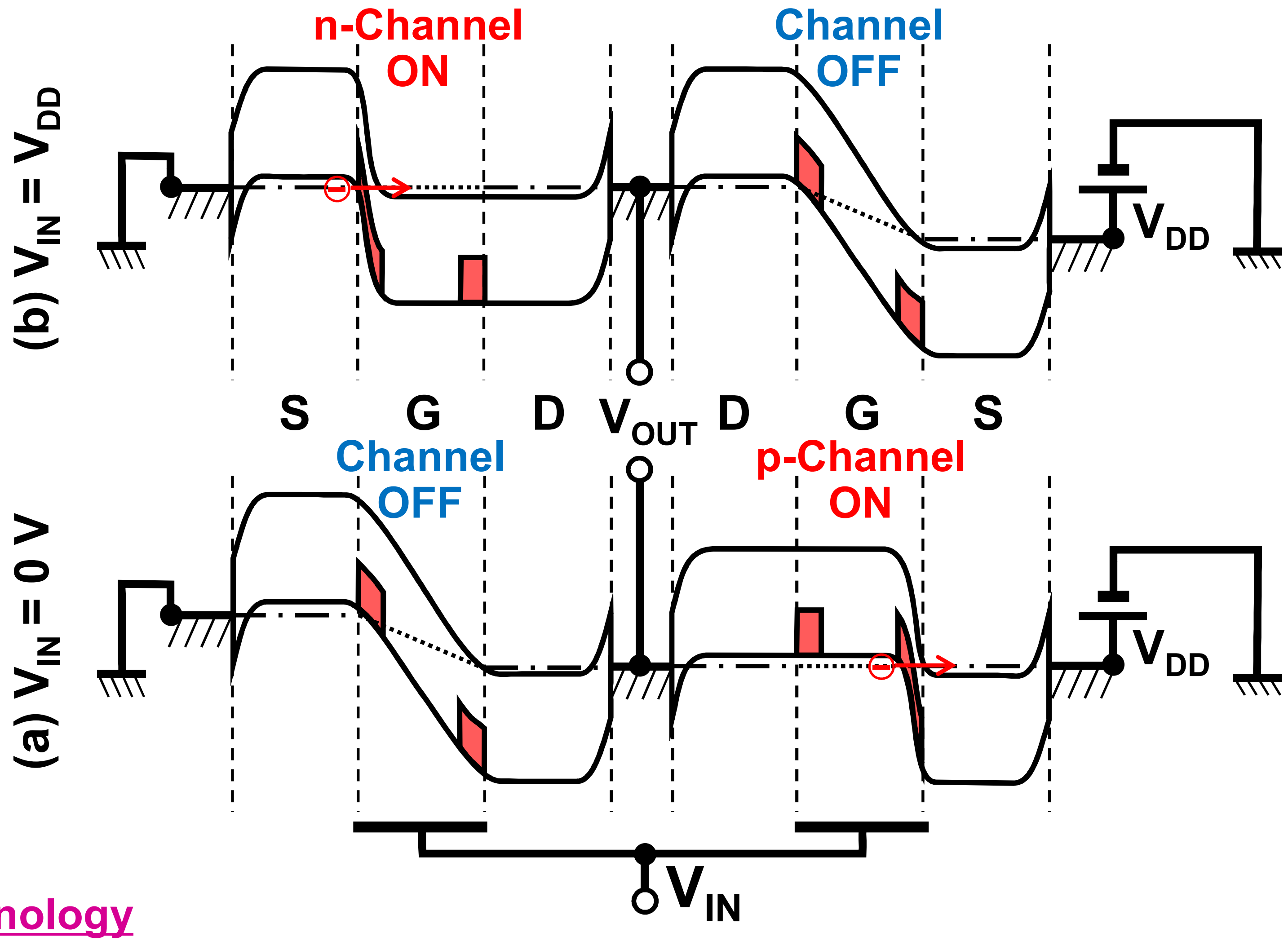


V_{Th} control by back-gate bias + Thinning channel fin (～10 nm)

→ Volume accumulation in n-/p-channel for improved current drivability

CMOS Inverter by Hetero-Tunnel Transistors (2)

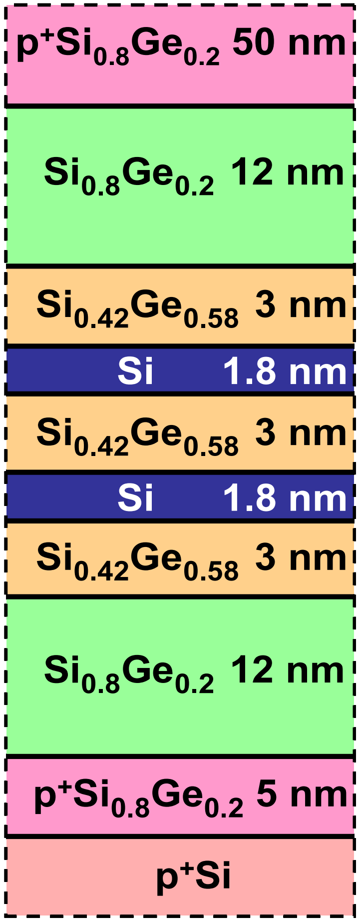
- Complementary switching by V_{Th} control with double gates
- Local reduction of effective bandgap by strained Si-C or Si-Ge-C alloy



Key Technology

Low-Temperature Epitaxial Growth／In-Situ Heavy Doping (Abrupt Interfaces)

Quantum Heterointegration Process of Highly Strained Group IV Semiconductors (1)



$p^+Si_{0.8}Ge_{0.2}$ 50 nm

$Si_{0.8}Ge_{0.2}$ 12 nm

$Si_{0.42}Ge_{0.58}$ 3 nm

Si 1.8 nm

$Si_{0.42}Ge_{0.58}$ 3 nm

Si 1.8 nm

$Si_{0.42}Ge_{0.58}$ 3 nm

$Si_{0.8}Ge_{0.2}$ 12 nm

$p^+Si_{0.8}Ge_{0.2}$ 5 nm

p^+Si

Si Barrier Growth

SiH_4 500°C

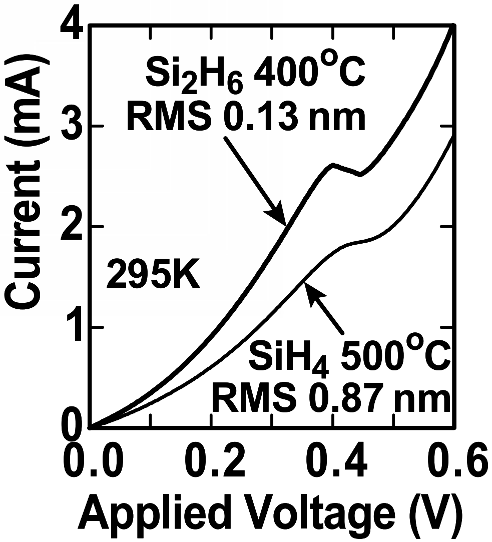
→ Si_2H_6 400°C

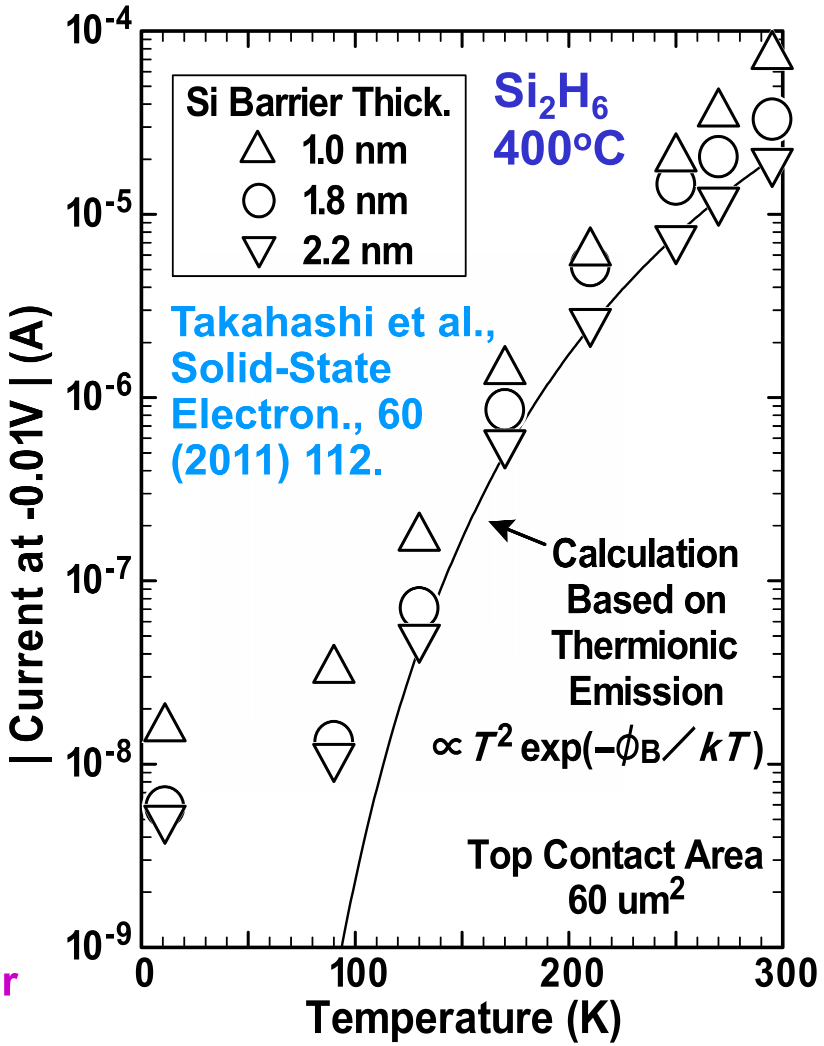
⇩

Interface Rough.

RMS 0.87 nm

→ 0.13 nm



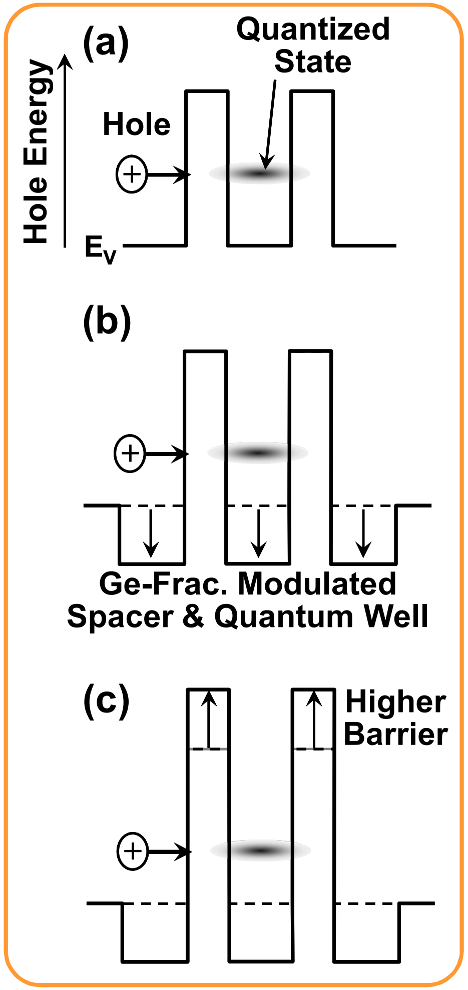


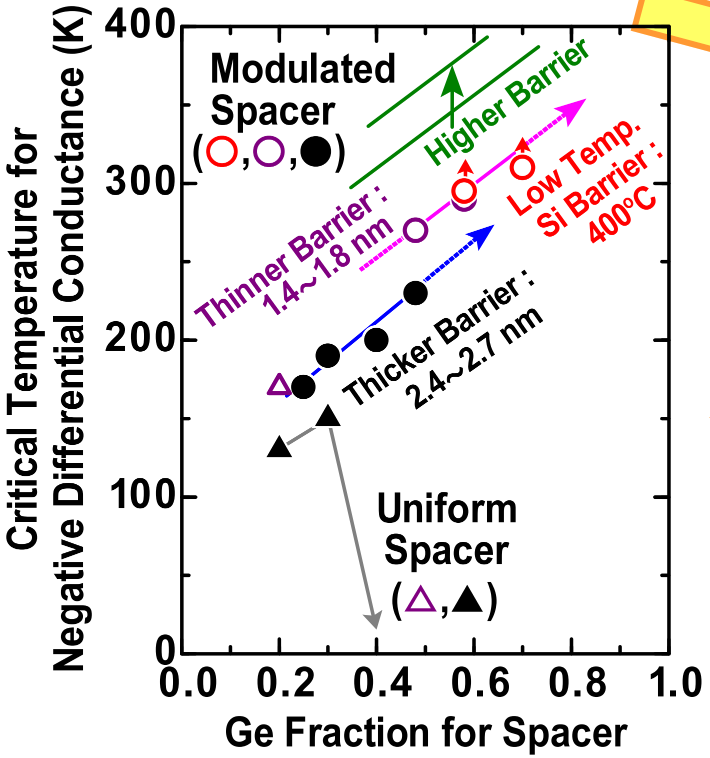
Takahashi et al., Solid-State Electron., 60 (2011) 112.

For Si-Ge resonant tunneling devices with higher performance, formation of heterostructure with nanometer-order thick films and control of atomic-order flatness are necessary. Moreover, exploring of higher barrier height materials for tunnel barriers is important.

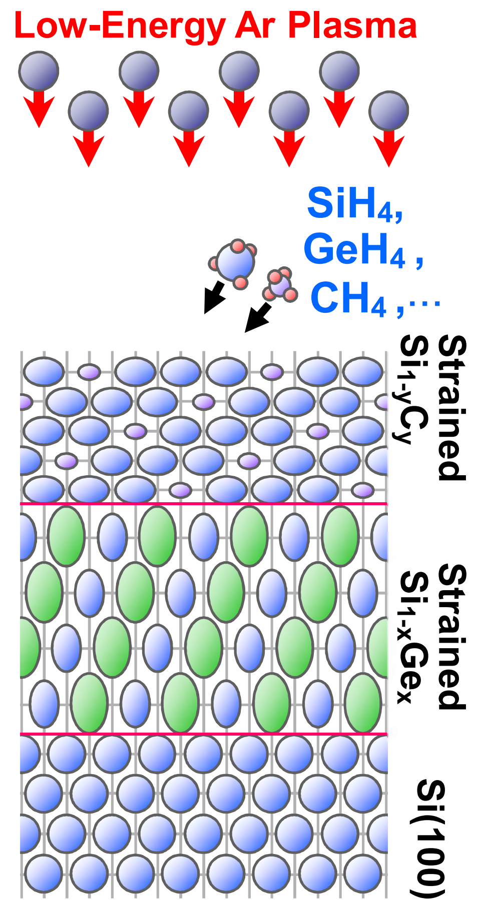
Quantum Heterointegration Process of Highly Strained Group IV Semiconductors (2)

- Surface reaction control of ultraclean reactant gases under low-damage and low-energy plasma without substrate heating
- Adsorption and reaction control by utilizing reactant gas activation (modification)
- Epitaxial growth of highly strained nanometer-order thin films out of thermal equilibrium





Expanding range of plasma condition for epitaxial growth



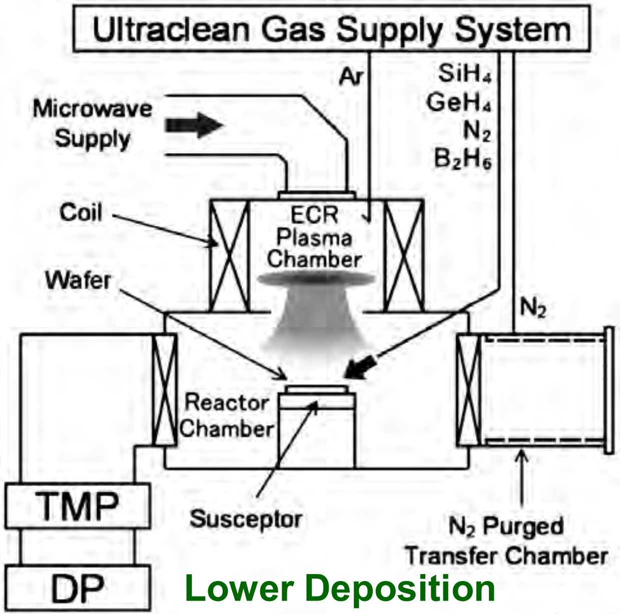
- Improvement of room-temp. resonant tunneling characteristics by utilizing highly strained nanometer-order thin films
- Establishment of heterointegration process of quantum-effect nanodevices

- Selective film formation (deposition and etching control) on upper surface and side-wall surface
- Epitaxial growth of highly doped nanometer-order thin films out of thermal equilibrium

Plasma CVD Processing for Group-IV Semiconductor Quantum Heterostructure

Key Eng. Mat., 470 (2011) 98

Low-Energy (<10 eV) Plasma Irradiation for Epitaxial Growth without Substrate Heating

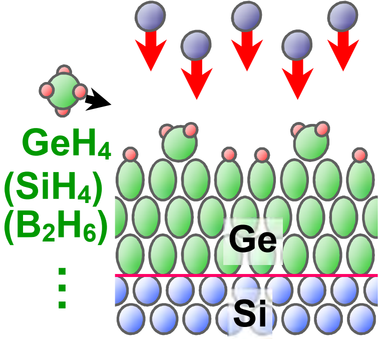


Lower Deposition Process below 100 °C can be enabled.

Low-Energy ECR Plasma CVD Apparatus

Lowering Surface Temp.
↓ (below 100 °C)
Suppresion of Islanding Growth
(Suppression of Plasma Damage)

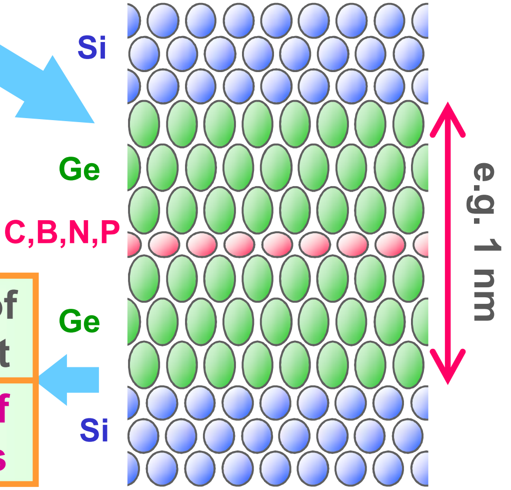
Low-Energy Ar Plasma



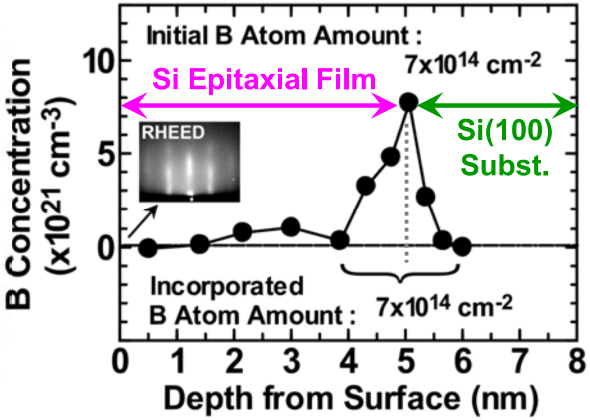
Enhancement of Quantum Effect

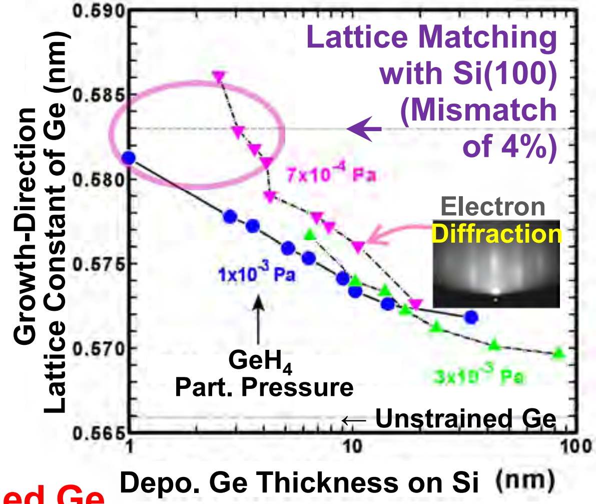
Investigation of New Properties

Nanometer-Order Strained Heterostructure with Modulation Doping
(Local Strain and Carriers, Ionized Impurity, ･･･)



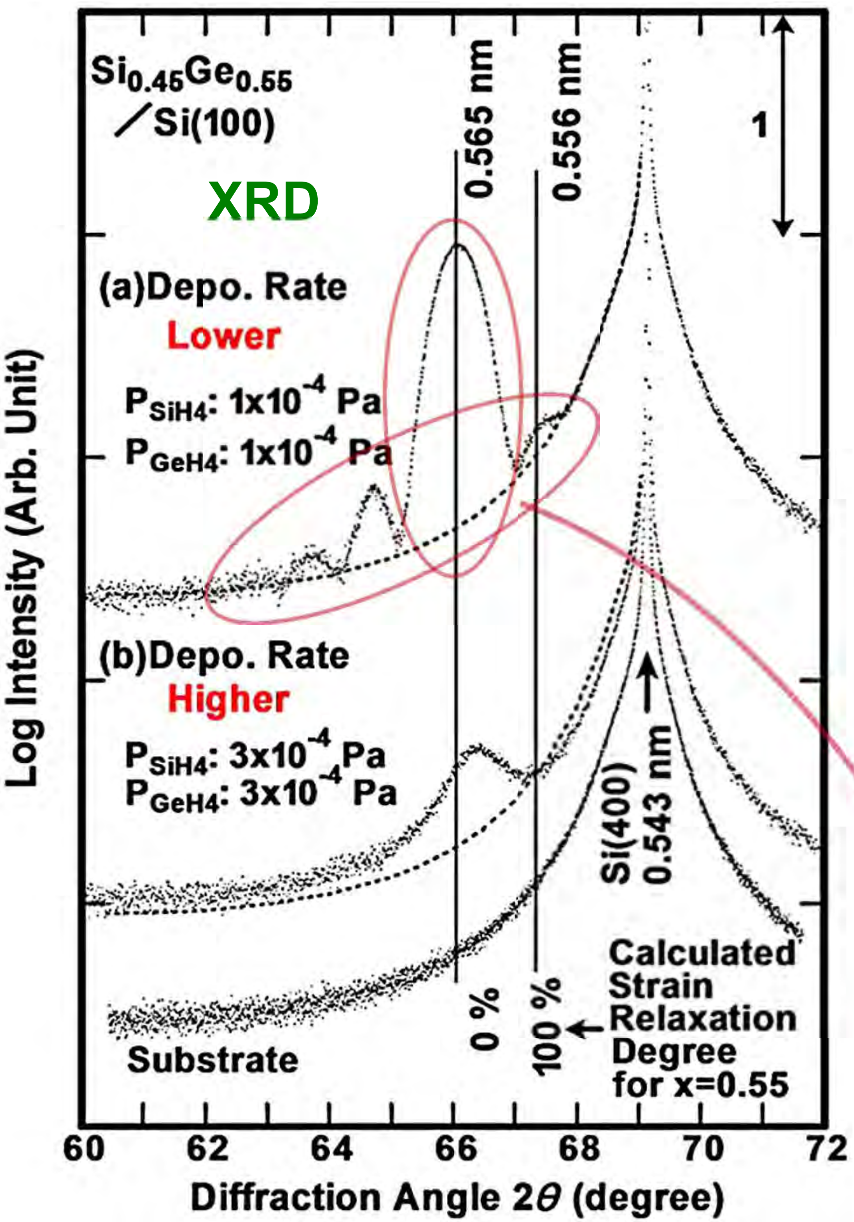
B Atomic-Layer Doping in Si





Epitaxial Growth of Highly Strained Ge

Strained Si-Ge Alloy Epitaxy on Si(100) w/o Subst. Heating



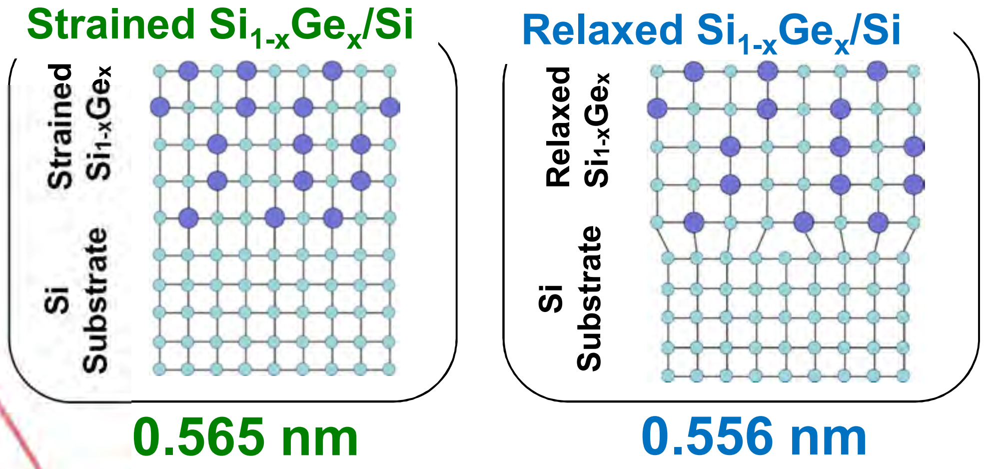
Thin Solid Films, 557 (2014) 31
ECS Trans., 64 (6) (2014) 99

Vertical Lattice constant at x = 0.55

$$0.556 - (2\, C_{12} / C_{11})\,(0.543 - 0.556)\ ;\ [\mathrm{nm}]$$

Elastic constants (Vegard's law)

$$C_{11} = 1.469,\ C_{12} = 0.559$$



Clear diffraction peak and thickness fringe pattern

Lattice constant of a flat 12 nm-thick $Si_{0.45}Ge_{0.55}$ film is almost matched with that of unstrained Si(100).